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COMPARATIVE STUDY OF 3-BIT, 4-BIT, 5-BIT AND 6-BIT CMOS FLASH ADC USING THE THRESHOLD INVERTER QUANTIZATION TECHNIQUE IN 0.250µM TECHNOLOGY

S. S. KHOT

Department of E & TC Engineering, Siddhant College of Engineering, Pune, Maharashtra, India

ABSTRACT

In this paper, an endeavour is fostered to the design and implementation of flash analog-to-digital converters (ADC), which are of high speed, low power, and low voltage. A comparison of 3-bit, 4-bit, 5-bit and 6-bit analog-to-digital convertors exercising the TIQ comparator with respect to speed and power at 3.3 V and 2.5 V respectively has been manifested. The threshold inverter quantization technique has been facilitated to attain the high speed in featured ADC while 0.250 µm CMOS technology has been facilitated to design a CMOS flash analog-to-digital convertor. The motive behind the use of this technique was to generate 2^n-1 different sized threshold inverter quantization comparators for an n-bit converter, so that the fast data conversion speed can be triumphed, which in turn can advance the operating speed and eliminate the ladder resistors that could lead to a significant reduction of power consumption. Further, two cascaded inverters as a voltage comparator have been facilitated. The gain boosters have been assisted to achieve the sharper thresholds for comparator outputs and a full digital output voltage swing. The thermometer codes (the outputs of comparator) have been converted to a binary code in two different steps through the encoder and '01' generator. Eventually, this paper proposed a flash ADC employing TIQ, which is designed by exercising FAT tree encoder that was simulated with the assistance to TANNER-EDA tool in 0.25 µm CMOS technology. The proposed flash ADC employing TIQ is appropriate and effectual for various System-on-Chip (SoC) applications.

KEYWORDS: Flash ADC, TIQ Comparator, Fat Tree Encoder, CMOS Technology, SoC Applications

INTRODUCTION

Analog to digital converters (ADC) interface with the real world analog signals, processing of digital signals and the computing world. Therefore, ADCs are considered the most important mixed signal circuits (Khot*et* al., 2012). The key parameters of an ADC are its speed, resolution and consumption of power (Yoo*et* al., 2002). Once ADC has been designed, these key parameters cannot be altered.

In this paper focuses on the design and implementation of flash analog-to-digital converters (ADC), which are of high speed, low power, and low voltage. A comparison of 3-bit, 4-bit, 5-bit and 6-bit analog-to-digital convertors exercising the TIQ comparator with respect to speed and power at 3.3 V and 2.5 V respectively has been manifested. The threshold inverter quantization technique has been facilitated to attain the high speed in featured ADC while 0.250 µm CMOS technology has been facilitated to design a CMOS flash analog-to-digital convertor. The motive behind the use of this technique was to generate 2^n-1 different sized threshold inverter quantization comparators for an n-bit converter, so that the fast data conversion speed can be triumphed, which in turn can advance the operating speed and eliminate the

ladder resistors that could lead to a significant reduction of power consumption. Further, two cascaded inverters as a voltage comparator have been facilitated. The gain boosters have been assisted to achieve the sharper thresholds for comparator outputs and a full digital output voltage swing. The thermometer codes (the outputs of comparator) have been converted to a binary code in two different steps through the encoder and '01' generator. A general optimisation has been done to achieve the lowest power consumption possible for the 2.5 V V_{DD}, 555 MHz A/D converters (Banik*et* al., 2011). Eventually, this paper proposed a flash ADC employing TIQ, which is designed by exercising FAT tree encoder that was simulated with the assistance to TANNER-EDA tool in 0.25 µm CMOS technology. The proposed flash ADC employing TIQ is appropriate and effectual for various System-on-Chip (SoC) applications.

THEORY OF ADC

The various types of ADCs have been studied in the literature, most notably are Flash ADC, Sigma delta ADC, Ramp counter ADC and Successive approximation ADC. However, the flash ADC architecture has been widely studied. It is faster due to its parallel architecture. That's why; it is also called as parallel ADC. It is exercised by comparing the analog signal (the input voltage) to a reference voltage that is maximum value achieved by the analog signal (Torres, 2006). For a ready reference the same can be understood by the following illustration. Suppose, the reference voltage is about 5 volts, means the peak of the analog signal will be 5 volts. When, the input signal will reach to 5 volts on an 8-bit ADC, we will get the maximum possible value on the ADC output i.e. 255 (11111111). Then, the reference voltage can be lowered through the register network and other comparators can be added to compare the analog signal (the input voltage) with other values (Khot*et* al., 2012; Torres, 2006).

A REVIEW OF RELATED WORK

A brief review of affixed work pertained to designing of a low power flash ADC exercisingTIQ has been manifested in this section. Yoo*et* al. (2001a) flourished acontemporary power saving design method for CMOS flash ADC. They employed the bisection method, in which only half of comparators in flash ADC functions in every clock cycle utilising NMOS and PMOS as switches along with an inverter as a comparator. Based on the results, they exhibited 6-bit flash ADC, which operates at 200MHz sampling rate and 3.3V supply voltage. Moreover, the use of power in this proposed circuit is only 40.75mW with HSPICE simulation. This bisection method by Yoo*et* al. (2001a) can reduce power consumption up to 43.18% as compared to the traditional flash ADC. Tsai (2004) evinced the design of an 8-bit FLASH Analog to Digital (A/D) Converter with Threshold Invert Quantization (TIQ) Comparators. They facilitatedthe power consumption at 800mW while the speed of this ADC at 787.78 Mbps. They designed and simulated individual blocks employing T-spice with 0.18 2m CMOS Technology. Rames and Gunavathi (2007) endeavoured a 4-bit and 1.8V Flash ADC design exercising500nm technology along with the CMOS-LTE Comparator. They generated the reference voltages with the help of transistors of the comparators by systematically sizing them. Therefore, for the architecture, they employed completely eliminating the resistive ladder network. As a result, they observe that the total power dissipation is 0.28753 mW.

Khot*et* al. (2012) presented a design and implementation of an ultrafast 3-bit 0.25µm CMOS Flash ADC based on TIQ comparator and concluded that the TIQ comparators based ADC is suitable for SoC applications and it is highly adaptable to future semiconductor technologies below 100 nanometers. Mohan and Ravisekhar (2014) proposed an efficient, low power encoding scheme intended for flash analog to digital convertor. To maintain the high speed with low

power dissipation, CMOS inverter has been used as a comparator. They proposed ADC is designed using 90n m technology in 1.2 V power supply using HSPICE tool.

For low power SoC application Kulkarni*et* al. (2010) schemed a 4-bit flash ADC. They employed a CMOS inverteras a comparator and adjusted the ratio of channel width and length. Moreover, to detect the input analog signal, they deviated the switching threshold of the CMOS inverter. The simulation results of their proposed 4-bit flash ADC flourished that the power consumption can be reduced about 78% compared to traditional flash ADC, if the process uses 3.3V supply voltage in TSMC 0.35 µmand uses about 12.4 mW at 200M sample. Rajshekhar and Bhatt (2008) and Yoo*et* al. (2001)materialised an ultrafast CMOS flash A/D converter design and exercised the featured A/D converterdesigned in CMOS. To achieve high-speed in CMOS,they exercised TIQ in featured A/D converter. They proposed a 6-bit TIQ based flash A/D converter, which is as per the parameters of 0.25m standard CMOS technology. This proposed flash A/D converter requires 0.013 mm^2 areas, dissipates 66.87mW of power at 2.5 V and operates with sampling rates up to 1 GSPS. This proposed flash A/D converter is appropriate for SOC applications in wireless products and other ultra-high speed applications.

TIQ FLASH ADC

The flash ADC advances the threshold inverter quantization (TIQ) technique for high speed, low power using standard CMOS technology and compatible with microprocessor fabrication (Rames and Gunavathi, 2007; Arakelyan, 2011; Khot*et* al., 2012). The block diagram of the TIQ flash ADC has been presented in figure 1.

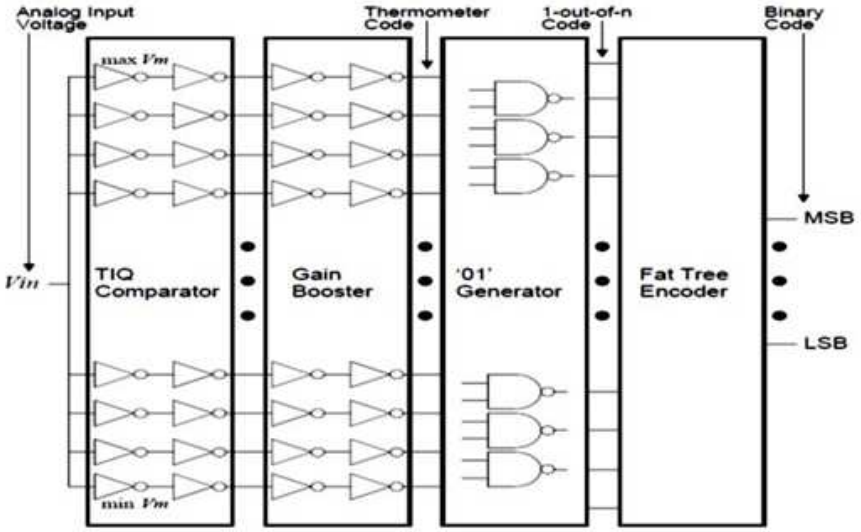


Figure 1: Block Diagram of ADC (Adopted from Banik*et* Al., 2011)

"The voltage comparators compare the input voltage with internal reference voltages, which are determined by the transistor sizes of the inverters." Therefore, the resistor ladder circuit used in a conventional flash ADC is not required in the design of TIQ Flash ADC (Rames and Gunavathi, 2007; Arakelyan, 2011; Mavani and Nandurbarkar, 2014).

The threshold inverter quantization (TIQ) is an innovative mechanism for generating a high speed CMOS flash ADC. The main difference between differential comparator and the TIQ comparator can be analysed through the way to supply their reference voltages. The differential comparator utilises the external reference voltage $V_r$using a resistor ladder circuit. The $V_r$directly depends on a resistor tap position. However, the TIQ comparator sets its switching threshold voltage

$V_m$internally as the built-in reference voltage, based on its transistor sizes. The TIQ based ADC employees the individual comparators in different sizes as compared to the traditional flash ADC, in which the identical in size comparators are exercised.2^n-1different inverters with different $V_m$value is required to design an n-bit flash TIQ based ADC and those must be arranged in the order of their $V_m$value (Khot*et* al., 2012).

Rames and Gunavathi (2007) stated that the TIQ comparator is a pure inverter circuit; it is faster and simpler than the differential comparator. It has the several advantages, most notably: the coupling capacitors, clock signals and switches are not necessary in the TIQ comparator when comparing the input voltage. It uses only usingtwo transistorsbetween the power supply rails in standard digital CMOS process, which makes this TIQ comparator most appropriate in SOC applications. The advanced CMOS technology below 0.1μm feature size and below 1.0 V power supply voltage is required to the TIQ comparator realisation(Yoo*et* al., 2002).

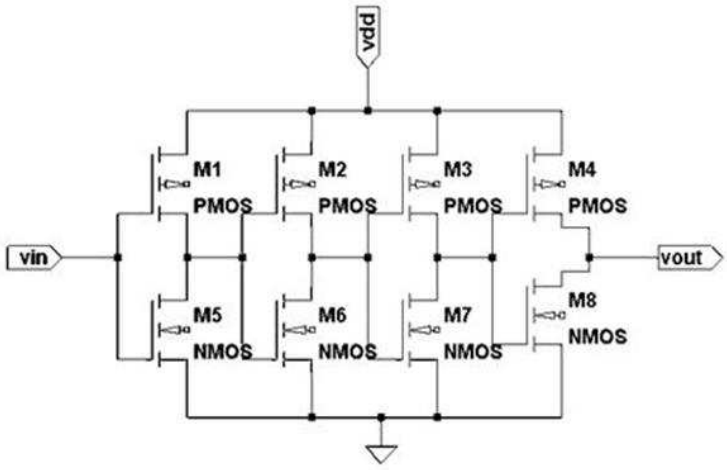


Figure 2: TIQ Comparator (Adopted from Ghai*et* al., 2007)

Kulkarni*et* al. (2010) and (Madankar and Palsodkar, 2013) stated that there are some basic problems with conventional comparator structures in Analog to Digital designs. Most notably: a large transistor area for higher accuracy is required, DC bias requirement, charge injection errors, metastability errors, high power consumption, and a resistor or capacitor array requirement. Yoo*et* al. (2001) suggested that these problems can be eliminated by using "Threshold Inverter Quantizer". The TIQ technique providesnumerousbenefits:the lower supply voltage,faster voltage comparison speed, simpler voltage comparator circuit, going to smaller feature size,eradication of resistor ladder circuit, highly adaptable to futurisms technology development andnot require switches, clock signal, or coupling capacitors for the voltage comparison,.

An output pattern named as a thermometer code is generated by comparatorsin a flash ADC. According to the thermometer code, the digital binary outputs are generated through bubble error corrector with an assistance of the encoder. The meta-stability errors can occur when the outputs of comparator are not known and passed through the ADC's encoder. Moreover, in flash ADC,the 2^n-1 comparators occupy a large area and usemore power Yoo*et* al. (2001). The TIQ comparator has a single ended input and is very sensitive to power supply noise Banik*et* al. (2011). The reference voltages are changed when there is a noise in the power supply voltage. To overcome this problem the CMOS Linear Tunable Trans conductance Element (CMOS-LTE) comparator has been proposed, which uses the TIQ comparator concept for the generation of reference voltages (Iyappan*et* al. 2009).

DESIGN OF ADC USING TIQ TECHNIQUE

The design of a flash ADC using TIQ technique is shown in Figure 1.

Design of TIQ Comparator Section

Ali and Choi (2001) stated the methods of optimal design and automation of the comparator circuit layout generation suitable a flash A/D converter. TIQ based A/D converters need 2^n-1 comparators and every individual must be different from all others. This method by Ali and Choi (2001) relevantlyembellishes the linearity of the A/D converter adversarial to the CMOSmechanismdigression.

As demonstrated in Figure 2, the TIQ comparator circuit encompasses four cascaded inverters. These four inverters are employed to bestow the sharper switching required for the comparator and also providing a full voltage swing. In a comparator, the same sizedPMOS and NMOS transistors can be employed; however they must be different for different comparators. These are depended on the switching voltage for which they have been designed. The mathematical equationfor the switching voltages can be given as:

$$V_{switching} = \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}}\left(V_{DD} - |V_{tp}|\right) + V_{tn}}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}}$$

(Adopted from Lee *et* al., 2002)

Where,

W_p= PMOS width,

W_n= NMOS width,

V_{DD}= Supply voltage,

V_{tn}= NMOS threshold voltage,

V_{tp}= PMOS threshold voltage,

μ_n= Electron mobility,

μ_p= Hole mobility,

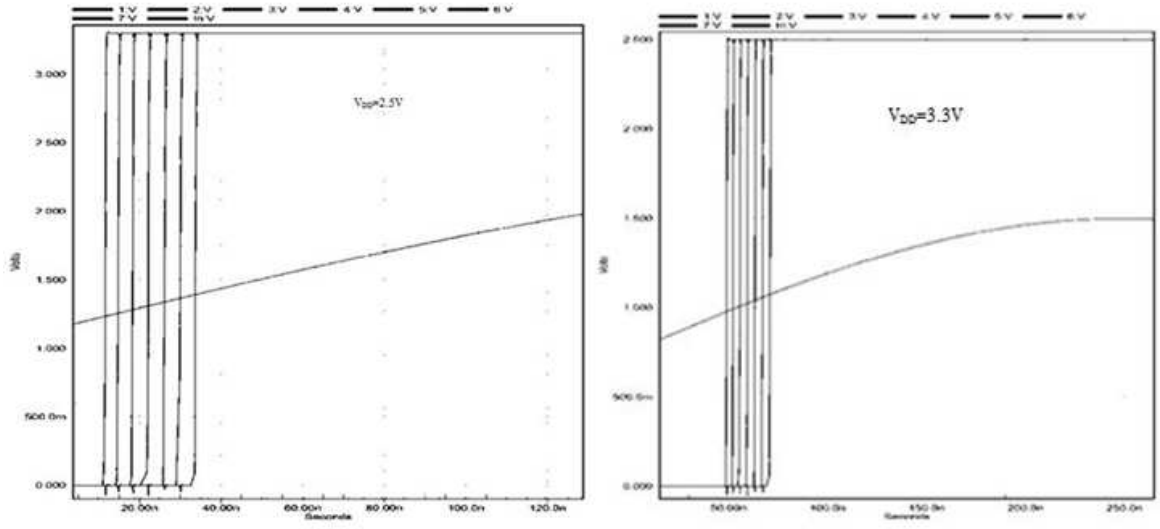
Assuming that PMOS length = NMOS length

The comparison voltage (i.e. Vm) changes with the help of varying the transistor sizes. While, the switching threshold voltage (i.e. Vm) for TIQ comparator is set internally as the built-in reference voltage on the basis of by transistor size. This TIQ based ADC employ the different sized individual comparators as compared to the conventional flash ADC, in which the identical in size comparators are employed. 2^n-1different inverters with different $V_m$value is required to design an n-bit flash TIQ based ADC and those must be arranged in the order of their $V_m$value. However, 63 individual TIQ comparators are required to construct a 6-bit ADC (Ghai*et* al., 2007; Lee *et* al., 2002; Khot*et* al., 2012).

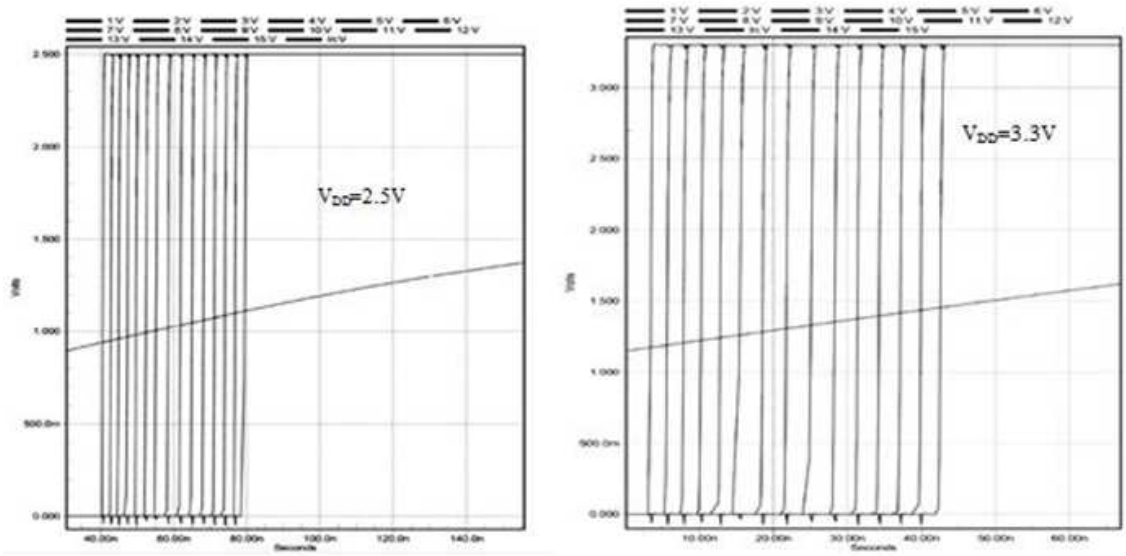
The comparators used in the system start switching on in succession mode as the input Analog voltage increases. As the output of the comparators the thermometer code is received. “The point where the code changes from one to zero is the point where the input signal becomes smaller than the respective comparator reference voltage levels.” This is known as thermometer code encoding (Madhumati*et* al., 2009).

Result of a TIQ Comparator

For n-bit Flash ADC we require 2n-1 TIQ comparators, so we require 7 comparators for 3-bit bit, 15 for 4-bit and 31 for 5-bit flash ADC design. For getting different switching voltages, the widths of PMOSare varied. The output results of the 3, 4, 5-bit TIQ comparator have been demonstrated in the Figure 3.



(a)



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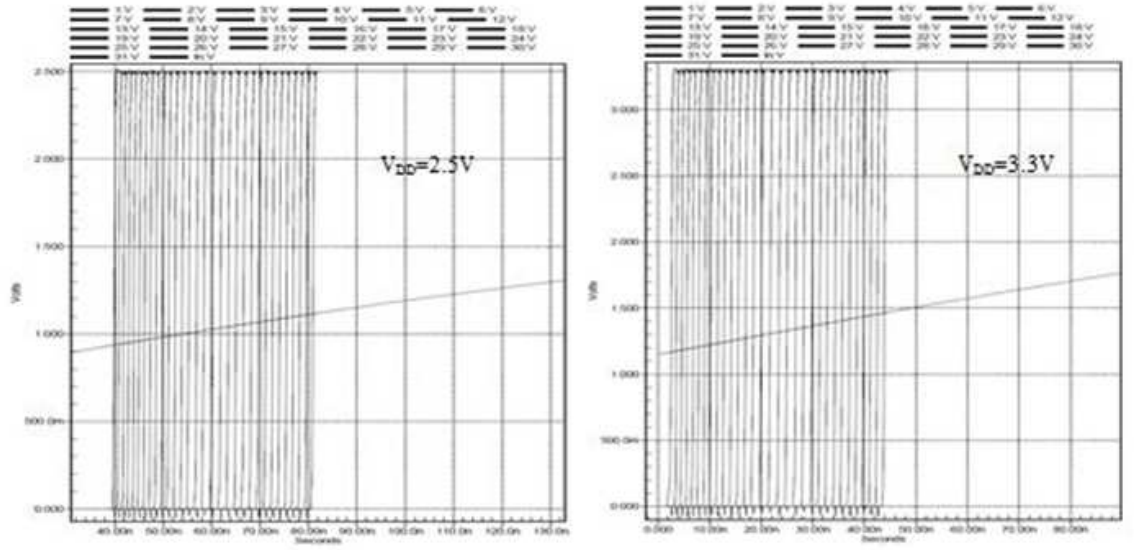
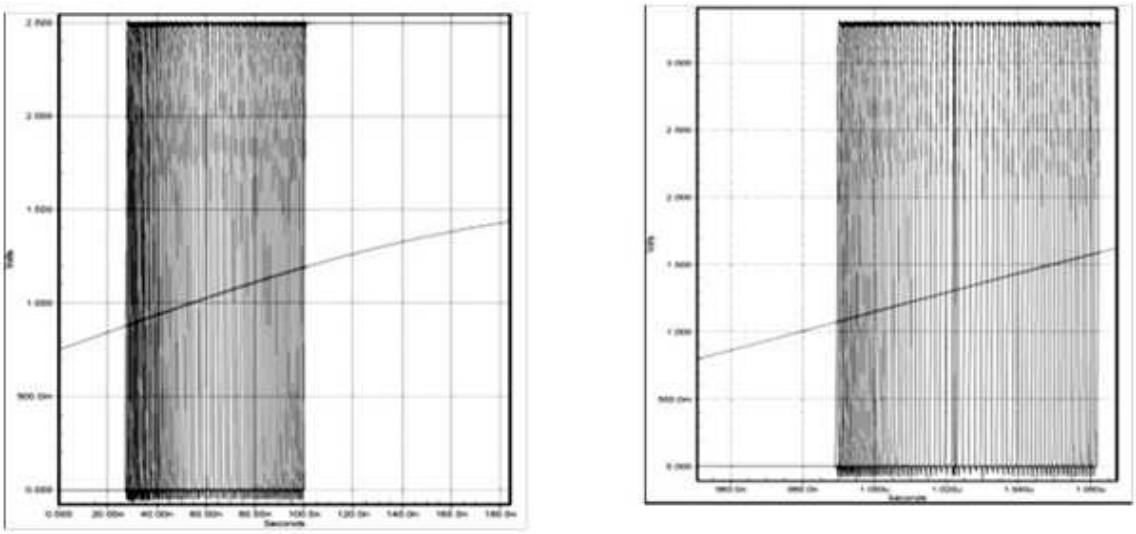


(c)



(d)

Figure 3: Switching of Various Comparators for (a) 3-Bit (b) 4-Bit (c) 5 Bit TIQ Flash ADC

Design of 1 Out of n Code Generator

The thermometer code, which is actually the output of the comparators in a flash ADC, is transmittedinto a binary code with the help of an encoder, in two different and simple steps. In first step, to get a '01' code, 1-out of n code generators are used to convert the thermometer code into a 1-out-of-n code. Then in second step, with the help of a fat tree encoder, '01' code is converted into a binary code (Chauhan*et* al., 2011).

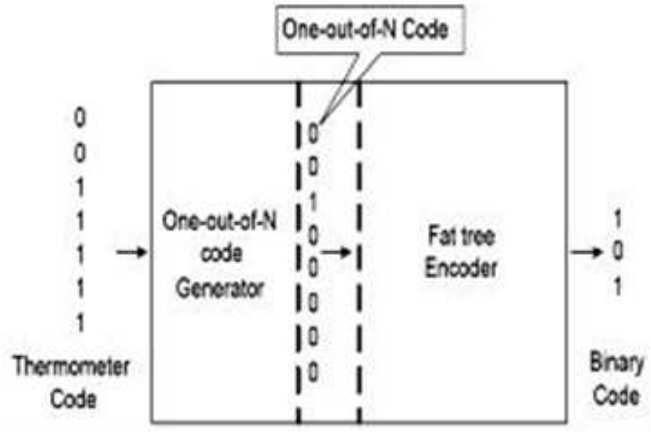


Figure 4: Two Stage Fat Treetc-BC Encoder (Adopted from Lee *et* al., 2002)

Fat Tree Encoder

For an ultra-high speed flash ADC, the thermometer code-to-binary code encoder is essential. In this research article, a fat tree thermometer code-to- binary code encoder has been proposed and presented that is highly suitable for the ultrahigh speed flash ADCs.

For the CMOS flash ADC,in terms of speed and power consumption, ROM encoder is outperformed by the fat tree encoder. By the fat tree encoder, the speed is enhanced by twice, which proves the fact that the fat tree encoder is an effective solution for an ultra-high speed ADC (Chauhan*et* al., 2011).

The TC (thermometer code)-to-BC (binary code) encoding is carried out in two stages in the fat tree encoder: the first stage converts the thermometer code to one-out-of-N code (Chauhan*et* al., 2011). This is shown in Fig.4. The one-out-of-N code is same as an address decoder output. This code conversion is done in N bit parallel using the gates. The second stage converts the one-out-of-N code to binary code using the multiple trees of OR gates shown in Figure 5 for 4-bit case.

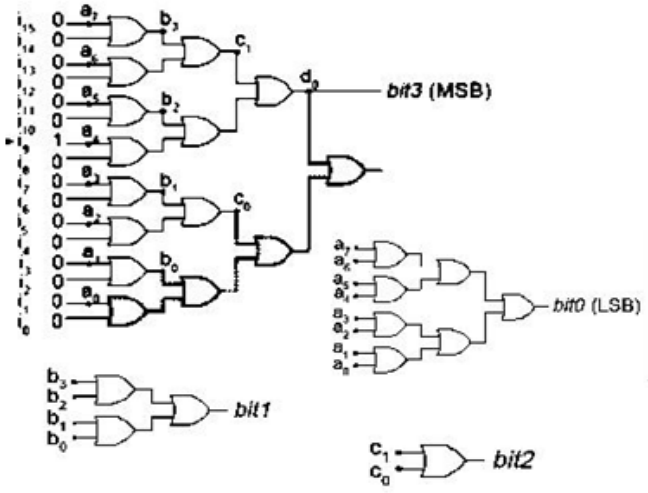


Figure 5: Fat Tree Encoder for 4-Bit (Adopted from Chauhan*et* al., 2011)

Design Steps

- In first step, exercising the HSPICE circuit simulator and substituting BSIM3 at Level 49 spice model test parameters; to verify the threshold voltage value of the midpoint quantizer (i.e. Qn) design a minimum size

inverter. However, during this design process, the channel length must be kept at the minimum value.

- In second step, forecast a safe analog input voltage range with the help of this eqatation: Analog range = Vdd - (VTN + | VTP|), where VTN and VTPare the threshold voltages for large NMOS and PMOS devices respectively,
- In third step, calculate the LSB value with following eqatation: LSB = Analog range/ 2n.

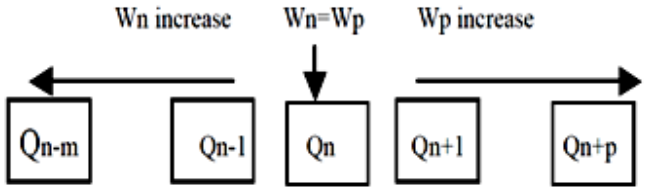
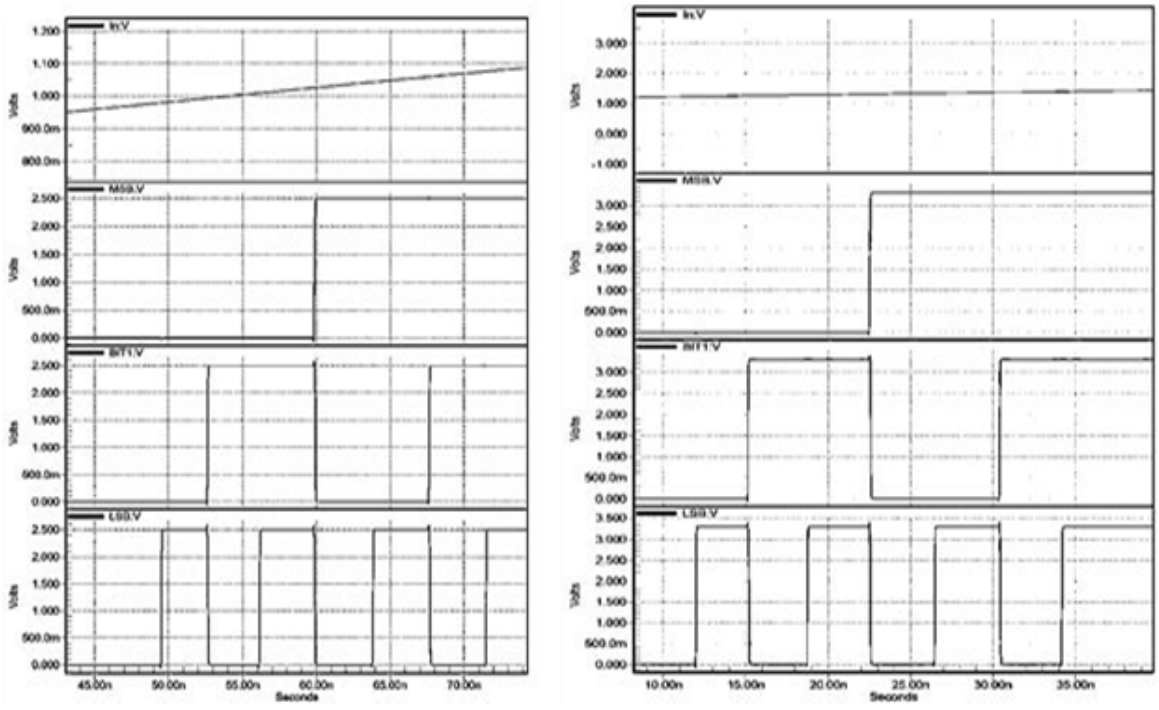


Figure 6: Block Diagram of a Design Process (Adopted from Kulkarni*et* al. 2010)

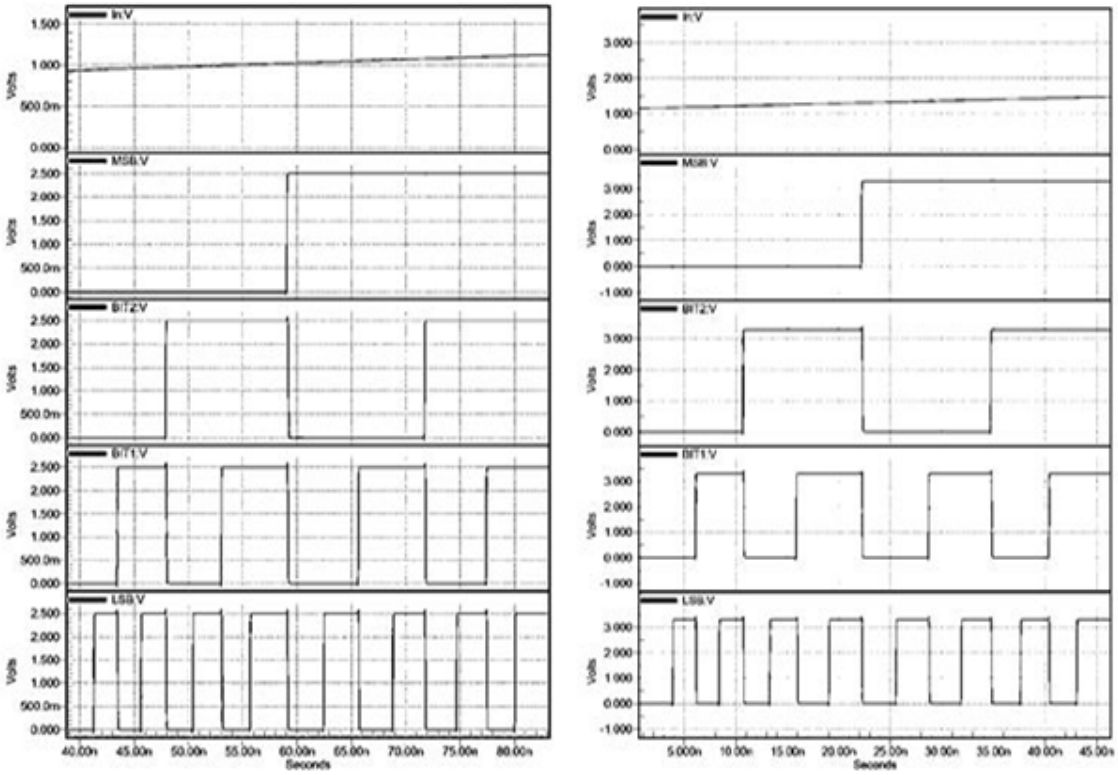
- In forth step, by assuming the midpoint value for Qn is in the center, calculate the ideal threshold points for each quantizer (Qn-m … Qn+p) accordingly.
- In last step, to get the corresponding closest possible channel widths, run the HSPICE simulator. The PMOS side, (W/L)n must be kept at the minimum valuefor the quantizers of Qn+1 … Qn+p), but to minimise the current flow during the transition of VTC,only the channel widths of the PMOS transistors can be changed. The same process can be applied to the NMOS side in the opposite way (Kulkarniet al. 2010)

SIMULATION AND RESULTS

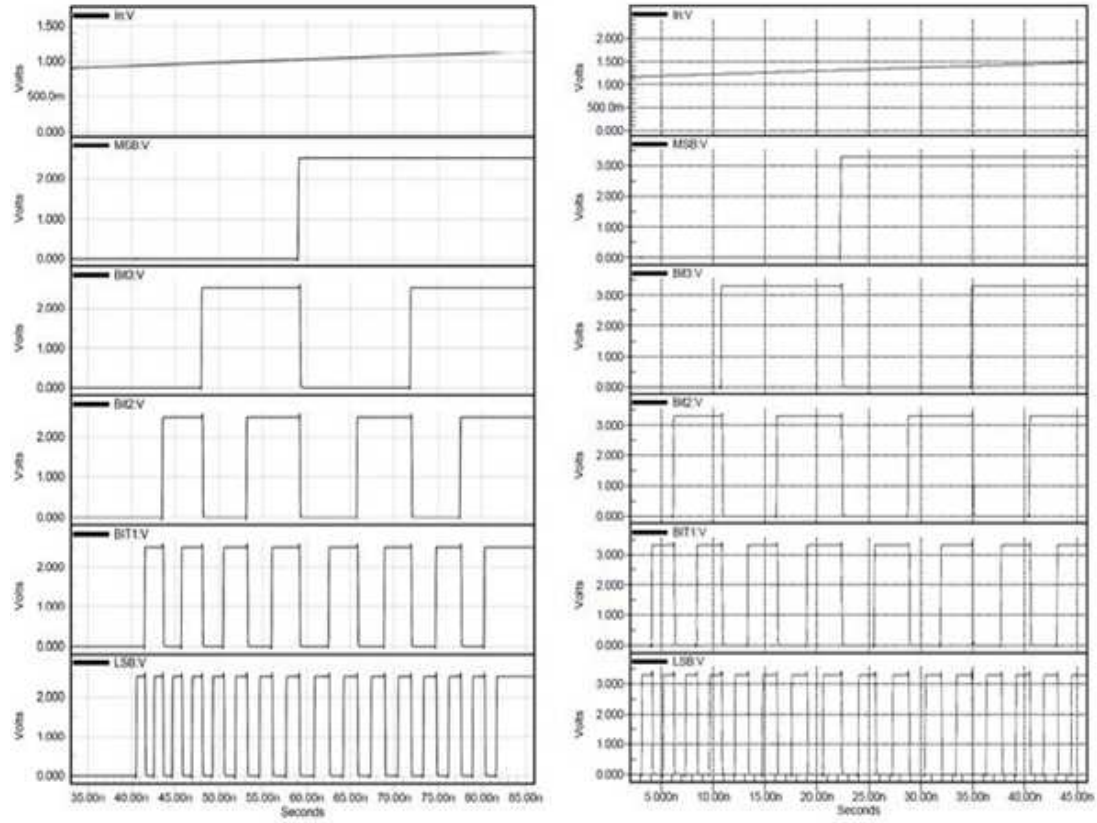
In the designing of flash ADC, TANNER-EDA tools are used to simulate the schematic circuit and obtain the result. After the schematic circuit is simulated using T-Spice tool of TANNER-EDA tool, the result of 3, 4, 5, 6-Bit flash ADC is obtained and is shown in Figure 6.



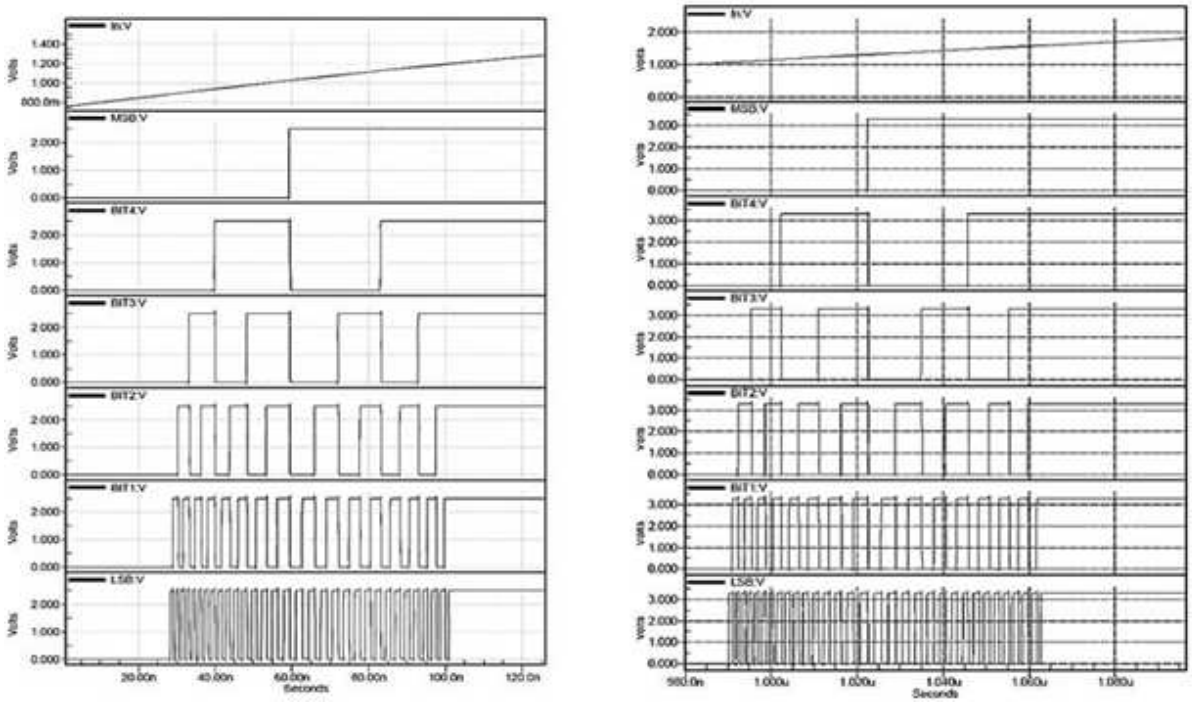
(a)


In:V
MSB:V
BIT2:V
BIT1:V
LSB:V
Volts
Seconds

(b)


In:V
MSB:V
BIT3:V
BIT2:V
BIT1:V
LSB:V
Volts
Seconds

(c)



(d)

Figure 6: Output of (a) 3-Bit (b) 4-Bit (c) 5-Bit (d) 6-Bit TIQ Flash ADC

CONCLUSIONS

Exercising TANNER-EDA tools, the design and simulation results of 3, 4, 5, 6-bit Flash ADC employing 0.25µm technology have been demonstrated in this paper. The power supply voltage given is 2.5 V and 3.3V. However, the circuit should be portable to smaller feature size CMOS technologies with lower supply voltages. The result is summarised in following table.

Table 1

Resolution (No. of Output Bits)	6-Bit		5-Bit		4-Bit		3-Bit	
CMOS Technology	0.250 µm		0.250 µm		0.250 µm		0.250 µm	
Transistor count	1928		942		436		202	
Power Supply (V_{DD})	2.5V	3.3V	2.5V	3.3V	2.5V	3.3V	2.5V	3.3V
Max Speed (MSPS)	500	565	555	628	555	690	588	781
Average Power Consumed (mW)	22.28	45.03	11.58	13.16	4.0890	9.98	4	9.74
Vm Range (Input Dynamic Range)	0.85V-1.2V	1.1V-1.6V	0.94V-1.12V	1.18V-1.48V	0.95V-1.15V	1.15V-1.45V	0.95V-1.15V	1.2V-1.4V
Vm Distance (V_{FSR}) (V)	0.35	0.5	0.00580	0.00967	0.01333	0.01333	0.02857	0.02857
V_{LSB}	0.00564	0.00806	0.000193V	0.00032V	0.00095 V	0.00095 V	0.004761V	0.004761V
Input signal frequency	1MHz							

It is important to notice that the proposed ADC in this paper is a clock less circuitry, which is a major cause of the less power consumption. Further, it has been planned to integrate the comparator exercising the latest CMOS technology for reducing the power consumption. Thus, an ADC which is functional at Nano scale CMOS technologies has been successfully designed and demonstrated. For designing a high-speed CMOS flash ADC, the major challenges can be listed as optimising the speed and power, static and dynamic offset reduction, calibration, and low supply voltage operation. The

design is targeted for applications such as high-speed serial links and UWB that require 4 bits of resolution at multi-GHz speeds.

The comparison of the results, collected from the different papers has been presented in the next table.

Table 2

Parameter	Resolution	Technology (µm)	Supply Voltage	Architecture Used	Power (mW)	Speed (MSPS)
Yoo*et* al. (2001a)	8-bit	0.250	2.5	TIQ	256	1000
Yoo*et* al. (2001)	6-bit	0.250	2.5V	TIQ Flash	66.87	1000
Ramesh and Gunavathi (2007)	8-bit	0.180	2.5V	TIQ flash	800	780
Celebi*et* al. (2005)	10-bit	0.500	1.5 V	Flash	250	500
Chauhan*et* al. (2011)	4-bit	0.350	3.3V	TIQ Flash	12.4	200
Proposed	**3-bit**	0.250	2.5V	TIQ Flash	4	9.74
Proposed	**3-bit**	0.250	3.3V	TIQ Flash	588	781
Proposed	**4-bit**	0.250	2.5V	TIQ Flash	4.089	555
Proposed	**4-bit**	0.250	3.3V	TIQ Flash	9.98	690
Proposed	**5-bit**	0.250	2.5V	TIQ Flash	11.58	555
Proposed	**5-bit**	0.250	3.3V	TIQ Flash	13.16	628
Proposed	**6-bit**	0.250	2.5V	TIQ Flash	22.28	500
Proposed	**6-bit**	0.250	3.3V	TIQ Flash	45.03	565

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